
IEEE Distinguished Lecturer Presentation hosted by the OTTAWA EMC chapter, and the Montreal EMC Chapter with Ottawa CPMT/ED/CAS/SSCS/AP/MTT Chapters as co-sponsors

Speaker : Dr. Wendem Beyene, Analog and Mixed Signal Architect, Facebook Inc.

Topic : Package Requirements for data rates of 112 Gbps and Beyond

Date : Wednesday, June 2, 2021

Time : 5:00 PM to 6:30 PM EST

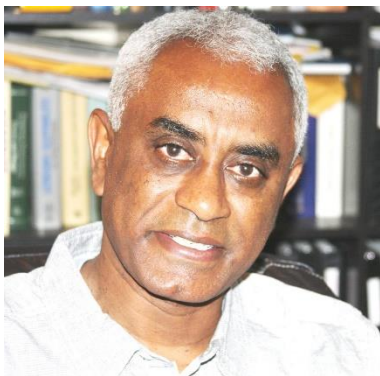
Location : Online via ZOOM (This presentation will NOT be recorded)

Registration: Free
Preference given to IEEE EMC CPMT/ED/CAS/SSCS/APS/MTT society members.
To register, please reply to this e-mail.

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Abstract: As the data rates increase rapidly in highspeed systems-- such as SerDes and memory systems-- to meet the bandwidth growth intensified by various applications, the electrical performance of packages has become critical. The bump and BGA or pin assignments, the layer stack up, and package material selection are very important to meet the signal and power integrity requirements. In addition, the role of new emerging 2.5D and 3D IC packaging platforms with ever increasing system integration requirements have made the role of packaging even more important. The sources of signal loss, noise coupling and discontinuities in packages must be fully understood and minimized when designing packages. At the same time, the design and development of packages have to meet cost, performance, form factor and reliability goals. In this talk we will examine the key electrical characteristics: signal loss, signal crosstalk, return loss, mode conversion, power integrity and other important factors necessary to meet the performance requirements of high-speed systems with data rates of 112 Gbps and beyond.

Biography:



Dr. Wendemagegnehu (Wendem) T. Beyene (M'88-SM'05) was born in Addis Ababa, Ethiopia. He received the B.S. and M.S. degrees in electrical engineering from Columbia University, New York, NY, USA, in 1988 and 1991, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, USA, in 1997. In the past, he was employed by IBM, Hewlett-Packard, and Agilent Technologies. In 2000, he joined Rambus Inc., Los Altos, CA, USA, and served as a senior principal engineer responsible for signal integrity of multi-gigabit parallel and serial interfaces. During 2017-2020 he served as principle engineer with responsible for signal and power integrity analysis of high-performance FPGA including fabric and high-speed I/O subsystems as well as I/O modeling. In 2020 he joined Facebook as a Analog & Mixed-Signal Architect

in Facebook Reality Lab.
Dr. Beyene has authored or co-authored numerous refereed publications in various leading IEEE Transactions and conferences. These publications covered various disciplines including package and interconnect modeling, analysis and optimization. He is currently an Associate Editor of IEEE Trans. On CPMT and is a Senior Member of Institute of Electrical and Electronic Engineers (IEEE). He also serves on several leading technical program committees, including EPEPS and SPI.