A Non-exhaustive List of Verilog HDL Resources[1]

Books

1. D.E. Thomas, P.R. Moorby, "The Verilog Hardware Description Language", Fourth Edition, Kluwer Academic Publishers, 1998, ISBN: 0-7923-8166-1, p.354, CD with VeryWell simulators, Synplicity FPGA Synthesis Software, examples from the book, and lecture slides.
2. S. Paltnikar, "Verilog HDL", SunSoft Press, A Prentice Hall Title, 1996, ISBN 0-13-451675-3, p.396, CD with SILOS III simulation environment for MS-Windows, Simucad Inc., demonstration version
3. J. Bhasker, "A Verilog HDL Primer", Second Edition, 1999, Star Galaxy Publishing, ISBN 0-9650391-7-X, p.294
4. J. Bhasker, "Verilog HDL Synthesis, A Practical Primer", 1998, Star Galaxy Publishing, ISBN 0-9650391-5-3, p.216
5. M.D. Ciletti, "Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL", 1999, Prentice Hall, ISBN 0-13-977398-3
6. M.D. Ciletti, "Advanced Digital Design with the Verilog HDL", Prentice Hall, 2002, ISBN: 0130891614
7. D.J. Smith, "HDL Chip Design, A practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs using VHDL or Verilog", 1996, 6th printing 2000, Doone Publications, ISBN 0-9651934-3-8
8. B. Zeidman, "Verilog Designer's Library", 1999, Prentice Hall, ISBN 0-13-081154-8
9. Z. Navabi, "Verilog Computer-Based Training Course", McGraw-Hill Publishing, 2002, ISBN: 0071374736
10. L. Bening, H. Foster, "Principles of Verifiable RTL Design", Kluwer Academic Publishers, 2001, ISBN: 0792373685
11. J. Bergeron, "Writing Testbenches, Functional Verification of HDL Models", 2000, Kluwer Academic Publishers, ISBN 0-7923-7766-4
12. 1364-2001 IEEE Standard for Verilog Hardware Description Language 2001, ISBN 0-7381-2827-9
13. S. Sutherland, "Verilog 2001: A Guide to the New Features of the VERILOG Hardware Description Language", Kluwer Academic Publishers, 2002, ISBN: 0792375688

Papers

1. S. Sutherland: "The IEEE Verilog 1364-2001 Standard - What's New, and Why You Need It", a white paper published in EE Times
   http://img.cmpnet.com/eedesign/features/Verilog-2001_paper.pdf
   Presentation slides for the white paper, presented at the International HDLCon conference in March, 2000
   http://www.verilog-2001.com/verilog-2001_presentation.pdf
2. S. Sutherland, D. Mills, "Getting the Most out of the New Verilog-2000 Standard", a white paper presented at the Synopsys Users Group (SNUG) Conference, 2001, in San Jose, California
   http://www.lcdm-eng.com/SJ_2001.pdf
3. C. Cummings: "Verilog 2001 Synthesis Enhancements", a white paper presented at the HDLCon Conference in March, 2001.
   http://www.sunburst-design.com/papers/CummingsHDLCON2001_Verilog2001_rev1_3.pdf

Tutorials

1. http://www.deeps.org/Verilog/veritut.html
2. http://www.aldec.com/Registration/(xanfcnyzedqam1yl2zxi4uua)/Download/Default.aspx?p=Verilog&v=Tutorial&platform=Windows
3. http://www.vol.webnexus.com/

Free Tools and Demos

1. Lattice ispLEVER Starter Software ispLEVER supports Verilog, VHDL, or Schematic/HDL (mixed mode) entry (downloading reqires opening a Lattice web account)
   http://www.latticesemi.com/products/devtools/software/ispLEVER-starter/index.cfm
2. Altera (downloading reqires registration)
   a) Quartus II Web Edition Software,
   b) MAX+PLUS II BASELINE & E+MAX Software
   c) LeonardoSpectrum-Altera Software
   http://www.altera.com/products/software/sfw-index.jsp
3. Xilinx ISE WebPACK 5.2i, for CPLD or medium-density FPGA designs (downloading reqires registration)
   http://www.xilinx.com/xlnx/xil_prodcat_landingpage.jsp?title=ISE+WebPack
4. Simucad, Silos Verilog Simulator (downloading reqires registration)
   http://www.silos.com/free_verilog_simulator/index.shtml
5. Icarus Verilog
   http://www.icarus.com/eda/verilog/
6. GPL Electronic Design Automation
   http://www.geda.seul.org/
7. Verilog.net Free Tools
   http://www.verilog.net/
8. Aldec's Active HDL Simulation and Design Entry Package (registration reqired)
   http://www.aldec.com/default.aspx

Training Courses

1. Esperan, the Methodology Training Company, "Verilog MasterClass, the Multimedia HDL Tutorial"
   http://www.esperan.com/mc_de.html
2. Altera Training Courses
   https://buy.altera.com/etraining/etraining.asp
3. Xilinx Training Courses
   http://www.xilinx.com/support/training/north-america-home-page.htm
4. Qualis Training and Library Resources
   http://www.qualis.com/cgi-bin/qualis/library.pl

User Groups

- Google Verilog Group: comp.lang.verilog
  http://groups.google.com/groups?hl=en&lr=&ie=UTF-8&oe=UTF-8&group=comp.lang.verilog
- Synopsys SolvNet Users Group: http://www.snug-universal.org/

Electronic newsletters

- ESNUG
  The ESNUG archive can be found at http://www.deepchip.com/esnug.html
  To subscribe send a request to mailto:esnug-request@world.std.com.
- Verification Guild
  The guild archive can be found at http://janick.bergeron.com/guild.
  To subscribe, simply send a request to janick@bergeron.com.

[1] This is an incomplete list of Verilog resources, which might be found helpful in increasing one's knowledge of Verilog. With the exception of reference [12], IEEE Standard 1364-2001 for Verilog, it is in no way approved or endorsed by IEEE. It is a sole responsibility of a reader to decide whether to use the resources listed.