IEEE CASS/EDS/SSCS Ottawa Joint Chapters, IEEE ComSoc/BTS/CES Ottawa Joint Chapter AP/MTT, CPMT and Computer Society & DoE-Carleton Joint Seminar (CASS Distinguished Lecture) are inviting all interested IEEE members and nonmembers to a seminar on

DL1: Title: Many-Core Chips: The New High-Performance Computing Platform

DL2: Title: Challenges for Electronics Design in the Nano-Scale

by

Prof. Yehea Ismail, Distinguished Lecturer, IEEE Circuits and Systems society, Dept. of EECS, Northwestern University, Evanston, IL60208-3118, USA

DATE: Tuesday February 28, 2012

TIME: DL1: 11:30AM - 12:30 p.m.; DL2: 12:30 p.m. – 01:30 p.m. Refreshments: Served

PLACE: ME 4124, Mackenzie Engineering Building, Carleton University, Ottawa, On., Canada

ADMISSION: Free. Registration required. To ensure a seat, please register by e-mail contacting: Ram Achar at achar@doe.carleton.ca, or Wahab Almuhtadi at almuhtadi@ieee.org.

Abstract

Abstract DL1: Many-Core Chips: The New High-Performance Computing Platform

Scaling as we know it is taking a different direction from the last three decades. Chips with tens of billions of transistors and hundreds of cores are expected to be the future of scaling. These chips will achieve performance through parallelism and application specific optimized cores. This trend will use superior technologies to integrate more cores on a chip rather than to push the frequency envelope as in the past. It is expected that every aspect of design and analysis will need to be modified to accommodate this new platform and trend. There is a clear need for new CAD tools and design methodologies that are very different from existing tools in both their focus and scope. This talk will delve into the specific challenges with respect to both design and CAD that is required for these many core chips. The talk will also provide an overview into the market and technology factors guiding and driving this trend. Attendees will be provided with insight into both present and future research vectors to support this nascent exponential.

Abstract DL2: Challenges for Electronics Design in the Nano-Scale

Semiconductor technologies exhibited explosive growth in complexity and speed over the last two decades. Since the early 1980s, the device sizes have scaled down from few micrometers to tens of Nano-meters and the operating frequencies have increased from a few megahertz to several gigahertz. Also, the spacing between devices and interconnect have dramatically decreased due to the continuous scaling down of the technology feature size. These trends have led to issues and challenges in the design and analysis of high performance integrated circuits that previous generations did not exhibit. Most of these issues are at the circuit and interconnect (physical) levels. Also, these issues are expected only to increase in importance in future generations of integrated circuits. This talk will overview the most important challenges for electronics design in the nano-scale.

Biography

Yehea Ismail (ismail@eecs.northwestern.edu) is the director of the Nanoelectronics Center at Northwestern University and the AUC. The center was inaugurated by Craig Barrett, Intel's chairman of the board in 2008, while in Nile University.

Professor Ismail is the Editor-in-Chief of the IEEE Transaction on Very Large Scale Integration (TVLSI) and the chair elect of the IEEE VLSI Technical Committee. He is on the editorial board of the Journal of Circuits, Systems, and Computers, was on the editorial board of the IEEE Transactions on Circuits and Systems I. Fundamental Theory and Applications, and a guest editor for a special issue of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems on “On-Chip Inductance in High Speed Integrated Circuits”. He has also chaired many conferences such as GLSVLSI, IWSOC,ISCAS. He is the Chief Scientist of the Innovation and Entrepreneurship Center of the Ministry of Communications and Information Technology, Egypt.

Professor Ismail has several awards such as the USA National Science Foundation Career award, the IEEE CAS outstanding author award, Best teacher award at Northwestern University, many best paper awards and teaching awards. Professor Ismail is the distinguished lecturer of IEEE CASS. He is an IEEE Fellow.

Professor Ismail has published more than 170 papers in the top refereed journals and conferences and many patents. He co-authored three books: On-Chip Inductance in High Speed Integrated Circuits, Handbook on Algorithms for VLSI Physical Design, and Temperature-Aware Computer Architecture. He has many patents in the area of high performance circuit and interconnect design and modeling. His work is some of the most highly cited in the VLSI area and is extensively used by industry.