

20th IEEE International Conference on Electrical Performance of Electronic Packaging and Systems EPEPS 2011

October 23-26, San Jose, CA, USA

Call for Papers

EPEPS is the premier international conference on advanced and emerging issues in electrical modeling, analysis, synthesis and design of electronic interconnections, packages and systems. It also focuses on new methodologies and CAD/design techniques for evaluating and ensuring signal, power and thermal integrity in high-speed designs. EPEPS is jointly sponsored by the IEEE Components, Packaging and Manufacturing Technology Society and IEEE Microwave Theory and Techniques Society. Authors are invited to submit papers describing **new technical contributions related to the broad area of electrical performance of high-speed designs**, covering:

- 1) Emerging and advanced issues,
- 2) New design techniques and innovative architectures for design and management,
- 3) Novel CAD concepts, methodologies and algorithms for modeling, simulation and optimization,

with emphasis on:

- System-level, board-level and on-chip interconnects
- High-speed channels, links, backplanes, serial and parallel interconnects, SerDes
- Multiconductor transmission lines
- Memory and DDR interfaces
- Jitter and noise management
- Signal and thermal integrity
- Power integrity and power distribution networks (PDNs)
- Electronic packages and microsystems
- 3D interconnects, 3D packages, TSVs and MCMs
- Nano interconnects and nano structures
- RF/microwave packaging structures, RFICs, mixed signal modules and wireless switches
- Package-chip co-design
- Electromagnetic (EM) and EM interference modeling, simulation algorithms, tools and flows
- Macromodeling and model order reduction as it applies to electrical analysis
- Advanced and parallel CAD techniques for signal, power and thermal integrity analysis
- Measurement and data analysis techniques for system-level and on-chip structures.

Technical Program Committee

Ramachandra Achar, Carleton University;
Henning Braunsch, Intel;
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Michel Nakhla, Carleton University;
Christopher Pan, Qualcomm;
Albert Ruehli, Emeritus IBM; Missouri U. S&T
Thomas-Michael Winkler, IBM;

Submission Deadline: July 01, 2011,
8pm, PST

Submission Format: 2 column, 4 page
pdf format only.

Information for authors can be found at www.epeps.org. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Noncompliant manuscripts will not be considered for review.

Location: Doubletree Hotel
2050 Gateway Pl, San Jose, USA

Tutorials/Workshops: EPEPS offers tutorials or short courses on state-of-the-art topics during the conference. Also on the first day (23rd Oct), a workshop entitled "*Future Directions in Packaging*" may be presented.

Exhibits: EPEPS offers an excellent array of vendor exhibits. EPEPS is an exciting forum for vendors to demonstrate their state-of-the-tools to the attendees. Interested vendors can contact the conference administration for more details.

Conference Co-chairs:

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Brian Young, Texas Instruments; brian.young@ti.com

For more information/contact:

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Conference Website:

www.epeps.org